



### N-Channel 100-V (D-S) MOSFET

#### CHARACTERISTICS

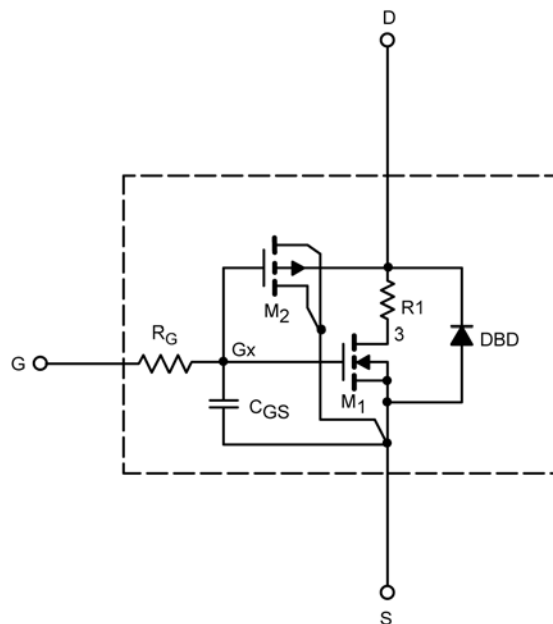
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model Si4102DY



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SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3		V
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.7 A	0.146	0.130	Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 2.5 A	0.154	0.145	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.7 A	8	7	S
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 2.1 A	0.82	0.80	V
<b>Dynamic<sup>b</sup></b>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	385	370	pF
Output Capacitance	C <sub>oss</sub>		39	40	
Reverse Transfer Capacitance	C <sub>rss</sub>		10	20	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.7 A	6.3	7.1	nC
			4.1	4.6	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 6 V, I <sub>D</sub> = 2.7 A	1.7	1.7	
Gate-Drain Charge	Q <sub>gd</sub>		1.8	2	

**Notes**

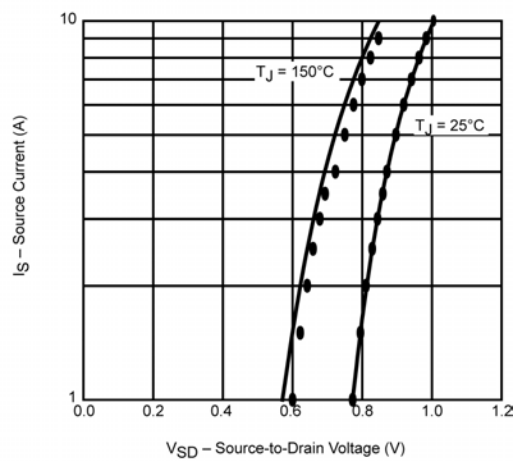
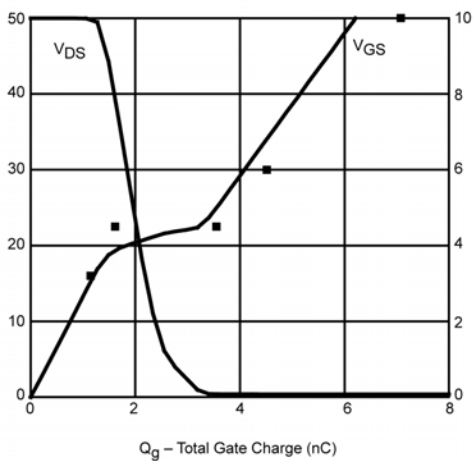
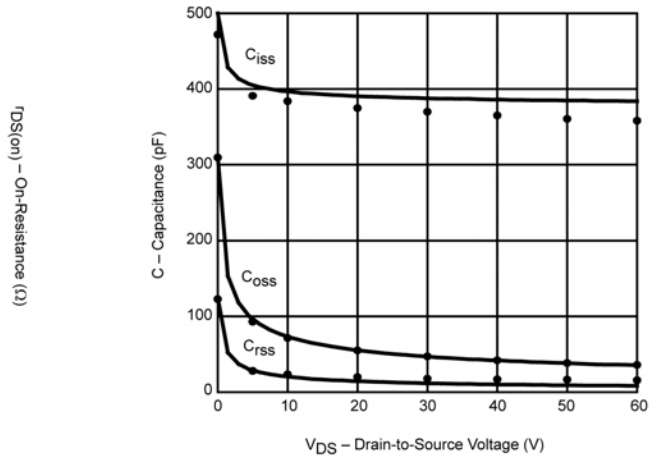
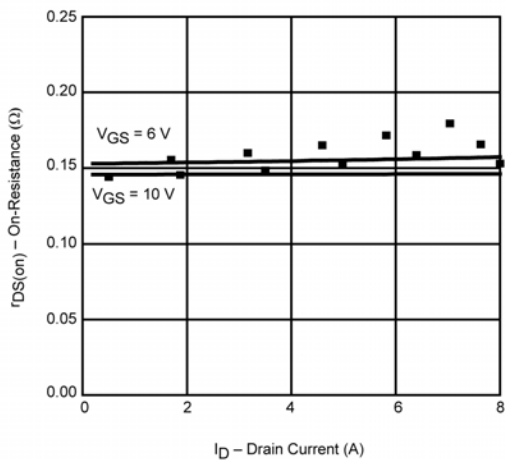
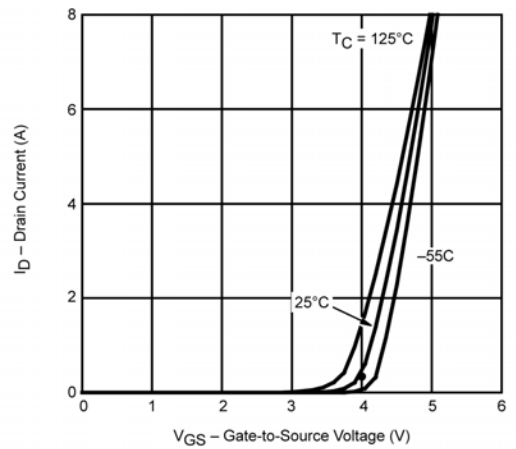
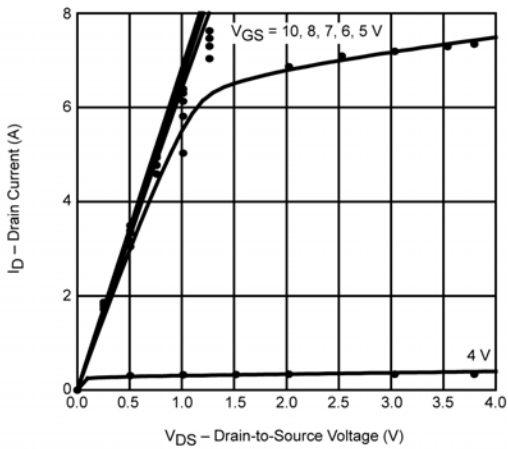
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



## Disclaimer

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